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Application Number	10/691,080 October 22, 2003		
Filing Date			
First Named Inventor	Barry E. Burke		
Art Unit	2818		
Examiner Name	C. Luu		
Attorney Docket Number	MIT8431L		

Examiner Initials*	Cite No.1	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	
iiiiais	NO.	Number-Kind Code ^{2 (f known)}	NAME OF THE	Applicant of Cited Document		
CAL	A1	^{US-} 3,728,590	04-17-1973	Kim et al.		
	A2	^{US-} 3,853,634	12-10-1974	Amelio et al.		
	A3	^{US-} 5,298,448	03-29-1994	Stevens et al.		
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		FOREIGN PATENT DOCU	MENTS	
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	Country Code ³ Number ⁴ Kind Code ⁵ (if kno	NA(71)		
xaminer			Date	12/22/4/

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Substitute for form 1449/PTO		Complete if Known			
				Application Number	10/691,080
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STA	STATEMENT BY APPLICANT		First Named Inventor	Barry E. Burke	
(Use as many sheets as necessary)		Art Unit	2818		
		Examiner Name	C. Luu		
Sheet	2	of	2	Attorney Docket Number	MIT8431L

	NON PATENT LITERATURE DOCUMENTS		
Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.		
B1	BROWNE et al., "A Nonoverlapping Gate Charge-Coupling Technology for Serial Memory and Signal Processing Applications," IEEE Jnl of Solid-State Circuits, Vol. SC11, No. 1, pp. 203-207, February 1976.		
B2	KAPOOR, "Charge-Coupled Devices with Submicron Gaps," IEEE Electron Device Ltrs., Vol. EDL-2, No. 4, pp. 92-94, April 1981.		
В3	SLOTBOOM et al., "Submicron CCD memory structures fabricated by electron-beam lithography," Proc. IEDM '84, paper 11.6, pp. 308-311, 1984.		
84	GAJAR et al., "An ionic liquid-channel field-effect transistor," J. Electrochem. Soc., V. 139, No. 10, pp. 2833-2840, October 1992.		
B5	YAMADA et al., "Driving Voltage Reduction in a Two-Phase CCD by Suppression of Potential Pockets in Inter-Electrode Gaps," IEEE Trans. on Electron Devices, V. 44, No. 10, pp. 1580-1587, October 1997.		
86	OKADA et al., "Performance of FT-CCD image sensor with Single Layer Poly-Silicon Electrode," 1999 IEEE Workshop on Charge-Coupled Devices and Advanced Imager Sensors, pp. 219-222, Nagano, Japan, June 1999.	·	
87	BURKE et al., "Charge-coupled device made with a single polysilicon level," Massachusetts Institute of Technology Lincoln Laboratory Solid State Research Quarterly Technical Report, pp. 31-37, March 1, 2002.		
	B1 B2 B3 B4 B5	Cite No.1 Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published. BROWNE et al., "A Nonoverlapping Gate Charge-Coupling Technology for Serial Memory and Signal Processing Applications," IEEE Jnl of Solid-State Circuits, Vol. SC11, No. 1, pp. 203-207, February 1976. KAPOOR, "Charge-Coupled Devices with Submicron Gaps," IEEE Electron Device Ltrs., Vol. EDL-2, No. 4, pp. 92-94, April 1981. SLOTBOOM et al., "Submicron CCD memory structures fabricated by electron-beam lithography," Proc. IEDM '84, paper 11.6, pp. 308-311, 1984. GAJAR et al., "An ionic liquid-channel field-effect transistor," J. Electrochem. Soc., V. 139, No. 10, pp. 2833-2840, October 1992. YAMADA et al., "Driving Voltage Reduction in a Two-Phase CCD by Suppression of Potential Pockets in Inter-Electrode Gaps," IEEE Trans. on Electron Devices, V. 44, No. 10, pp. 1580-1587, October 1997. OKADA et al., "Performance of FT-CCD image sensor with Single Layer Poly-Silicon Electrode," 1999 IEEE Workshop on Charge-Coupled Devices and Advanced Imager Sensors, pp. 219-222, Nagano, Japan, June 1999. BURKE et al., "Charge-coupled device made with a single polysilicon level," Massachusetts Institute of	

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